The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A die-level opto-electronic device, comprising:

a semiconductor die formed substantially from a semiconductor material and having edges and a photonic device optically exposed on a first surface;

a conductive structure formed in **a depression in the semiconductor material** and **extending** through at least a portion of the semiconductor material of the die and not on the side edges of the semiconductor material of the die, the conductive structure **having,**

a conductive layer having two surfaces on opposing sides of the layer, a top surface and a bottom surface, the bottom surface in contact with the depression in the semiconductor material,

a support feature formed in the depression on the top surface of the conductive layer and formed of dielectric material, and

the bottom surface of the conductive layer being exposed on a second surface of the die that opposes the first surface, wherein the conductive structure is electrically connected to the photonic device; and

an optically transparent laminate attached to the first surface so as to overlay the photonic device.

2. (Original) The die-level opto-electronic device of claim 1 wherein the photonic device is an image sensor.

3. (Original) The die-level opto-electronic device of claim 1 further comprising an under bump metallization pad attached to the second surface, the under bump metallization pad being electrically connected to the conductive structure.

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4. (Original) The die-level opto-electronic device of claim 3 wherein the under bump metallization pad is redistributed so as to occupy a different location on the second surface than the conductive structure.

5. (Original) The die-level opto-electronic device of claim 1 further comprising a solder bump deposited on the conductive structure so as to extend beyond the second surface.

6. (Original) The die-level opto-electronic device of claim 1 wherein the optically transparent laminate comprises a glass.

7. (Currently Amended) A semiconductor wafer, comprising:

a substrate formed substantially from a semiconductor material and having a plurality of photonic devices optically exposed on a first surface;

a plurality of conductive structures formed in **a plurality of depressions in the semiconductor material** and **extending** through at least a portion of the semiconductor material of the substrate, the plurality of structures **each having,**

a conductive layer with two surfaces arranged on opposing sides of the layer, a top surface and a bottom surface, the bottom surface in contact with an associated depression in the semiconductor material,

a support feature formed in the depression on the top surface of the conductive layer and formed of dielectric material, and

the bottom surface of each conductive layer being exposed on a second surface of the substrate that opposes the first surface, wherein ones of the plurality of structures are electrically connected to associated ones of the plurality of photonic devices; and

an optically transparent laminate attached to the first surface so as to overlay the plurality of photonic devices.

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8. (Original) The semiconductor wafer of claim 7 wherein the plurality of photonic devices further comprises a plurality of image sensors.

9. (Original) The semiconductor wafer of claim 7 further comprising a plurality of under bump metallization pads attached to the second surface, ones of the plurality of under bump metallization pads being electrically connected to associated ones of the plurality of conductive structures.

10. (Original) The semiconductor wafer of claim 9 wherein the plurality of under bump metallization pads is redistributed so as to occupy different locations on the second surface than the plurality of conductive structures.

11. (Original) The semiconductor wafer of claim 7 further comprising a plurality of solder bumps, wherein ones of the plurality of solder bumps are deposited on associated ones of the plurality of conductive structures so as to extend beyond the second surface.

12. (Original) The semiconductor wafer of claim 7 wherein the optically transparent laminate comprises a glass.

Claims 13-20 (Canceled).

21. (New) The device of claim 1 further comprising a bond pad formed on the first surface overlaying a portion of the conductive structure.

22. (New) The semiconductor wafer of claim 7 further comprising a plurality of bond pads formed on the first surface wherein each bond pad overlies a portion of ones of the conductive structures.

23. (New) A die-level opto-electronic device, comprising:

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a semiconductor die formed substantially from a semiconductor material and having edges and a photonic device optically exposed on a first surface, the die further including apertures in the first surface of the die;

a conductive structure formed in the aperture extending through at least a portion of the semiconductor material of the die and not on the side edges of the semiconductor material of the die, the conductive structure having,

a conductive layer having two surfaces on opposing sides of the layer, a top surface and a bottom surface, the bottom surface in contact with inner walls of the aperture,

a support feature formed of dielectric material formed in the aperture, and

the bottom surface of the conductive layer being exposed on a second surface of the die that opposes the first surface, wherein the conductive structure is electrically connected to the photonic device; and

an optically transparent covering that overlays the photonic device.

24. (New) The device of Claim 23 wherein the aperture of the first surface of the die has a spherically contoured sidewall.

25. (New) The device of Claim 23 wherein the conductive structure of the first surface of the die extends below the second surface of the die.

26. (New) The device of Claim 23 further comprising a solder bump deposited on the conductive structure.

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